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A Novel Hybrid Dstatcom Topology for Load Compensation with Non-Stiff Source

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ABSTRACT
The distribution static compensator (DSTATCOM) is a shunt active filter, which injects currents into the point of common coupling (PCC) (the common point where load, source, and DSTATCOM are connected) such that the harmonic filtering, power factor correction, and load balancing can be achieved. The distribution static compensator (DSTATCOM) is used for load compensation in power distribution network. A new topology for DSTATCOM applications with non-stiff source is proposed. The proposed topology enables DSTATCOM to have a reduced dc-link voltage without compromising the compensation capability. It uses a series capacitor along with the interfacing inductor and a shunt filter capacitor. With the reduction in dc-link voltage, the average switching frequency of the insulated gate bipolar transistor switches of the D-STATCOM is also reduced. Consequently, the switching losses in the inverter are reduced. Detailed design aspects of the series and shunt capacitors are discussed in this paper. A simulation study of the proposed topology has been carried out using MATLAB environment and the results analyzed.
Keywords **–** Dc link voltage, distribution static compensator (DSTATCOM), hybrid topology, nonstiff source.

I. INTRODUCTION

The proliferation of the power electronics-based equipment, nonlinear and unbalanced loads, has aggravated the power quality (PQ) problems in the power distribution network. They cause excessive neutral currents, over heating of electrical apparatus, poor power factor, voltage distortion, and high levels of neutral –to-ground voltage, and inference with communication systems. The literature records the evolution of different custom power devices to mitigate the power-quality problems by injecting the voltages/currents or both in to the system. The shunt connected custom power device, called the distribution static compensator (DSTATCOM), injects current at the point of common coupling (PCC) so that harmonic filtering, power factor correction, and load balancing can be achieved. The DSTATCOM consists of a current-controlled voltage source inverter (VSI) which injects current at the PCC through the interface inductor. The operation of VSI is supported by a dc storage capacitor with proper dc voltage across it. One important aspect of the compensation is the extraction of reference currents. Various control algorithms are available in literature to compute the reference compensator currents. However, due to simplicity in formulation and no confusion regarding the definition of powers, the control algorithm based on instantaneous symmetrical component theory is preferred. Based on algorithm, compensator reference currents are given as follows:

P_{lavg}

$$\left.\begin{aligned} i_{fa}^{*} &= i_{la} - \{(v_{sa} + \gamma(v_{sb} - v_{sc}))(P_{lavg} + P_{dc})/(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)\} \\ i_{fb}^{*} &= i_{lb} - \{(v_{sb} + \gamma(v_{sc} - v_{sa}))(P_{lavg} + P_{dc})/(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)\} \\ i_{fc}^{*} &= i_{ic} - \{(v_{sc} + \gamma(v_{sa} - v_{sb}))(P_{lavg} + P_{dc})/(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)\} \end{aligned}\right\}$$

Where =tanφ/√3 and φ is the desired phase angle between the supply voltages and compensated source currents in the respective phases. For unity power factor operation, φ=0, thus □ =0. The term P_{lavg} is the dc or average value of the load power. The term P_{dc} in the above equations accounts for the losses in the VSI without any dc loads in its dc link. To generate, a P_{dc} suitable closed loop dc link voltage controller should be used, which will regulate the dc voltage to the reference value.

For the DSTATCOM compensating unbalanced and nonlinear loads, the transient performance of the compensator is decided by the computation time of average load power and losses in the compensator. In most DSTATCOM applications, losses in the VSI are a fraction of average load power. Therefore, the transient performance of the compensator mostly depends on the computation of P_{lavg}. In this paper P_{lavg}, is computed by using a moving average filter (MAF) to ensure fast dynamic response. The settling time of the MAF is a half-cycle period in case of odd harmonics and one cycle period in case of even harmonics present in voltages and currents. Although the computation of is generally slow and updated once or twice in a cycle, being a small value

compared to it does not play a significant role in transient performance of the compensator.

when the dc link of the DSTATCOM supplies the dc load as well, the corresponding dc power is comparable to the average load power and hence plays a major role in the transient response of the compensator. Hence there are two important issues. The first one is the regulation of the dc link voltage with prescribed limits under transient load conditions. The second one is the settling time of the dc link voltage controller. Conventionally, a PI controller is used to maintain the dc link voltage. It uses the deviation of the capacitor voltage from its reference value as its input. However, the transient response of the conventional dc-link voltage controllers is slow especially in the applications where the load changes rapidly. Some work related to the dc link voltage controllers and their stability is reported in [16]-[20]. However work is limited to rectifier units where switching patterns are well defined and analysis can be easily carried out. In this paper, a fast acting dc link voltage controller based on dc link capacitor energy is proposed. The detailed modeling, simulation and experimental verifications are given to prove the efficacy of this fast acting dc link voltage controller. There is no systematic procedure to design the gains of the conventional PI controller used to regulate the dc link voltage of the DSTATCOM. Herewith, mathematical equations are given to design the gains of the conventional controller based on the fast acting dc link voltage controller to achieve similar fast transient response.

II. DSTATCOM FOR COMPENSATING AC AND DC LOADS

Various VSI topologies are described in the literature for realizing the DSTATCOM to compensate unbalanced and nonlinear loads [21]-[29]. Due to the simplicity, the absence of the unbalance in the dc link voltage and independent current tracking with respect to other phases, a three phase H-Bridge VSI topology is chosen. The following figure.1: shows a three phase-four-wire-compensated system using H-bridge VSI topology-based DSTATCOM compensating unbalanced and nonlinear ac load.

A dc load () is connected across the dc link. The DSTATCOM consists of 12 insulated-gate bipolar transistor(IGBT) switches each with an antiparallel diode, dc strorage capacitor, three isolation transformers and three interface conductors.The statr point of the isolation transformers() is connected to the neutral of load() and source (N). The H-bridge VSIs are connected to the PCC through interface inductors. The isolation transformers prevent a short circuit of the dc capacitor for various combinations of switching states of the VSI. The inductance and resistance of the isolation transformers are also included in and . The source voltages are assumed to be balanced and sinusoidal. With this supply being considered as a stiff source, the feeder impedance(-) shown in the above figure.1: is negligible and hence it is not accounted in state-space modelling. To track the desired compensator currents, the VSIs operate under the hysterisis band current control mode due to their simplicity, fast response, and being independent of the load parameters [30]. The DSTATCOM injects currents in to the PCC in such a way as to cancel unbalance and harmonics in the load currents. The VSI operation is supported by the dc storage capacitor with voltage across it. The dc bus voltage has two functions, that is, to support the compensator operationand to supply dc load. While compensating, the DSTATCOM mantains the balanced sinusoidal source currents with unity power factor and supplies the dc load through its dc bus

III. STATE-SPACE MODEL OF THE DSTATCOM

For the DSTATCOM topology shown in the above Figure.1: the pairs of switches $S_{1a}S_{2a}$ and $S_{4a}S_{3a}$ are always ON and OFF in complimentary mode. The ON and OFF states of these switches are represented by a binary logic variable S_a and its complementS_a'. Thus when switches $S_{1a}S_{2a}$ are ON, it implies that switches $S_{4a}S_{3a}$ are OFF. This is represented by S_a=1, S_a'=0, and vice-versa. In a similar way S_b,S_b', and S_c &S_c' represent gating signals for switches S_{1b}-S_{2b},S_{3b}-S_{4b},S_{1c}-S_{2c},S_{4c}-S_{3c}, respectively. Using the notations for the system shown in the above figure the state-space equations are written as follows:

$$X' = \mathbf{Ax} + \mathbf{Bu} \quad (2)$$

Where state vector **x** and input vector **u** are given by

$$\mathbf{x} = [i_{fa}\ i_{fb}\ i_{fc} V_{dc}]^T \quad (3)$$

$$\mathbf{u} = [V_{sa}\ V_{sb}\ V_{sc}]^T \quad (4)$$

here **T** is the transpose operator.

System matrix [**A]** and input matrix [**B**] ,[1]-[10]

IV. SELECTION OF THE DC-LINK CAPACITOR

The value of the dc-link capacitor can be selected based on its ability to regulate the voltage under transient conditions. Let us assume that the compensator in figure.1 is connected to a system with the rating of X kilovolt amperes. The energy of the system is given by X × 1000J/s. Let us further assume that the compensator deals with half (that is X/2) and twice (that is 2X) capacity under the transient conditions for n cycles with the system voltage period of T s. Then, the change in energy to be with by the dc capacitor is given as $\Delta E = (2X - X/2)nT$

Now this change in energy (21) should be supported by the energy stored in the dc capacitor. Let us allow the dc capacitor to change its total dc-

link voltage from 1.4Vm to 1.8Vm during the transient conditions where is the peak value of the phase voltage.

Table:SYSTEM PARAMETERS

System Quantities	Values
System voltages	230 V (line to neutral), 50 Hz
Feeder impedance	$Z_s = 1 + j3.141\ \Omega$
Linear load	$Z_{la} = 34 + j47.5\ \Omega$, $Z_{lb} = 81 + j39.6\ \Omega$, $Z_{lc} = 31.5 + j70.9\ \Omega$
Nonlinear load	Three phase full bridge rectifier load feeding a R-L load of 150 Ω-300 mH
VSI parameters	C_{dc}=3300 μF, V_{dcref}= 1.6V_m= 520 V, L_f= 26 mH, R_f= 0.1 Ω
PI controller gains	K_p=2, K_i=0.5
Hysteresis band (h)	± 0.5 A

V. Results and Discussions

The load compensator with H-bridge VSI topology as shown in figure.1 is realized by digital simulation by using MATLAB. The load and the compensator are connected at the PCC. The ac load consists of a three phase unbalanced load and a three phase diode bridge rectifier feeding a highly inductive R-L load. A dc load is realized by an equivalent resistance () as shown in the figure. The dc load forms 50% of the total power requirement. The system and compensator parameters are given in table1. By monitoring the load currents and PCC voltages, the average load power is computed. At every zero crossing of phase a voltage, is generated by using the dc-link voltage controller. The state space equations are solved to compute the actual compensator currents and dc-link voltage. These actual currents are compared with the reference currents given by (1) using hysteresis current control. Based on the comparison, switching signals are generated to compute the actual state-variables by solving the state-space model given in (2). The source voltages and load currents are plotted in figure 4(a) and (b). The load currents have total harmonic distortions of 8.9%, 14.3%, and 21.5% in phases a, b and c, respectively. The unbalance in load currents results in neutral current as illustrated in the figure. The compensator currents and compensated source currents are shown in Figure 4 and (d). As seen from figure 4(d), the source currents are balanced sinusoids; however, the switching frequency components are superimposed over the reference currents due to the switching action of VSI. The currents have a unity power factor relationship with voltages in the respective phases.

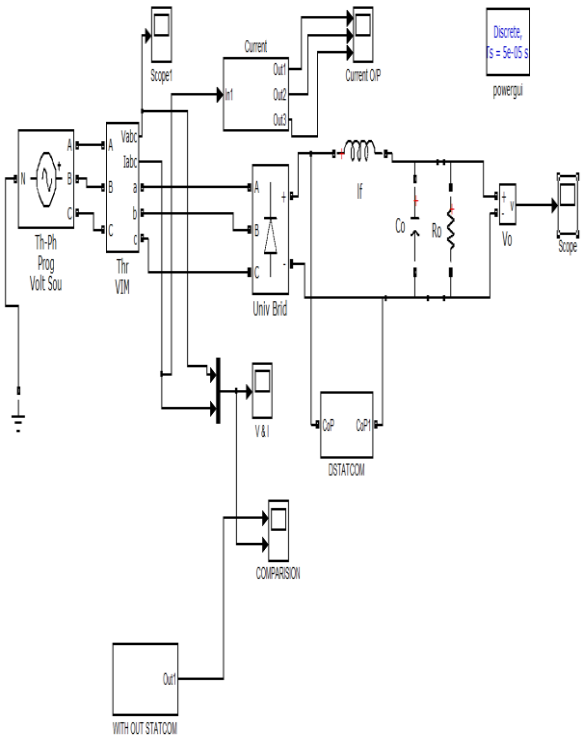

Fig: Simulation diagram for Proposed DSATCOM Technique

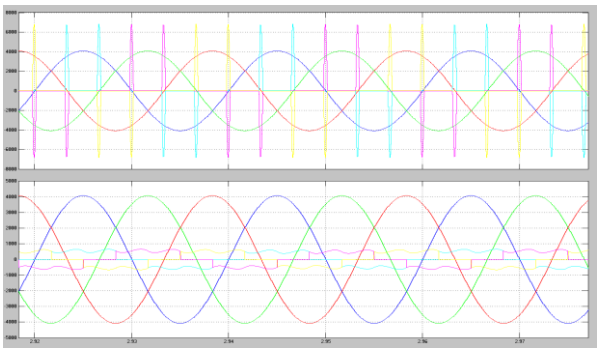

Fig: Output Voltage wave forms

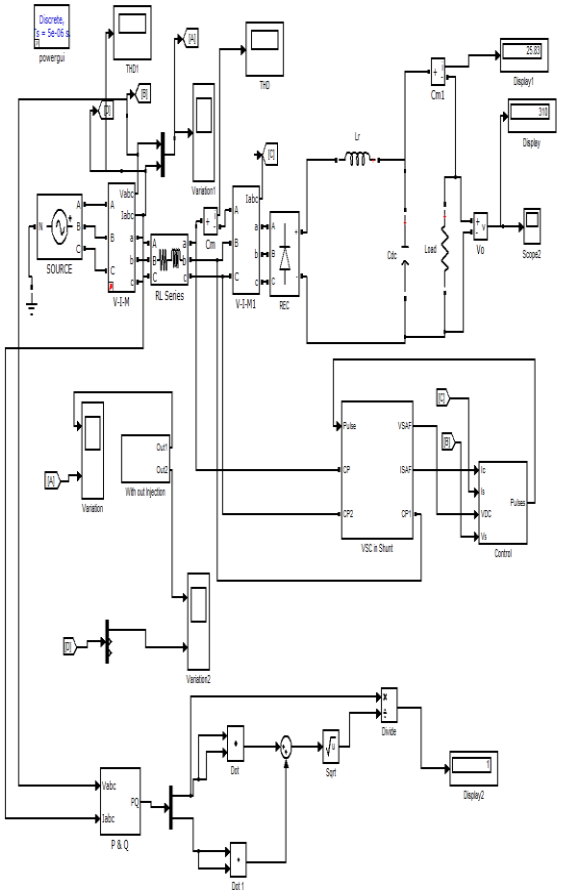

Fig: Simulation Diagram for Closed Loop V& I control of Proposed DSTATCOM Technique

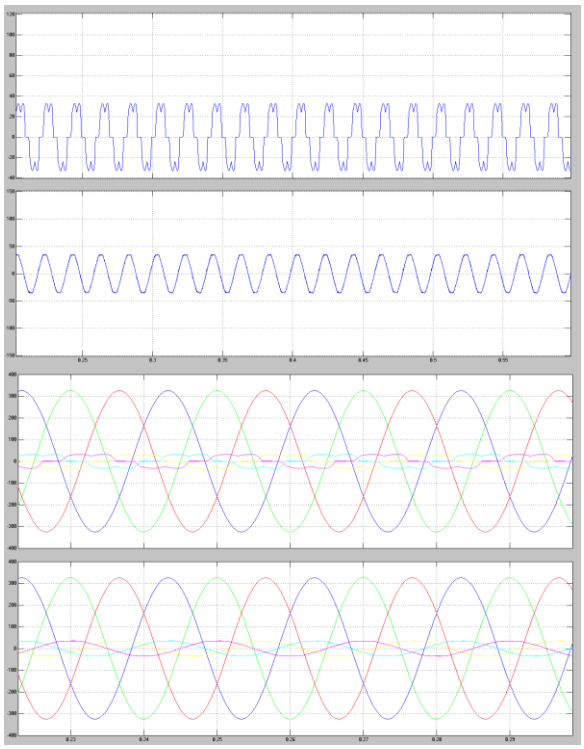

Fig: Output waveforms of Currents and voltages

VI. CONCLUSIONS

A new hybrid DSTATCOM topology has been proposed in this paper, which has the capability of compensating the load at a lower dc-link voltage under non stiff source. Design of the filter parameters is explained in detail. The proposed method is validated through simulation and experimental studies in a 3-□ distribution system with the neutral clamped DSTATCOM topology. Detailed comparative studies are made for the conventional and proposed hybrid DSTATCOM topologies. From this study, it is found that the proposed topology has less average Switching frequency, less THDs in the source currents and terminal voltages with reduced dc-link voltage as compared to the conventional DSTATCOM topology.

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